

# A Computer-Operated Manufacturing and Test System

**Abstract:** A computer system utilizing duplexed central processors and three types of satellite computer terminals has been developed for the control of manufacturing processes and product tests. The system was designed for use in a plant producing data processing equipment. The prime objectives of the project were (1) to reduce the time required for the plant to accept new products or product changes, (2) to reduce control and test equipment costs by using standard control and test equipment, and (3) to improve product quality through more uniform processes and tests. The objectives were met by using small, stored-program computer terminals to control individual tests and processes. These terminals are connected to a central computer system which assists with data processing and serves as an input/output device for the terminals.

The design and implementation of the system occurred in two phases. During the first phase the stored-program test terminal, a high-speed data transmission system, and a multiplexer were designed and installed on an IBM 1460 Data Processing System. A programming system was developed concurrently with the hardware. This system included a real-time monitor and application and utility programs which were written for operation in a time-shared environment. During the second phase of development a process control terminal, a data acquisition terminal, and a new multiplexer for duplexing two 1460 Data Processing Systems were designed and implemented. Also developed were shared file control units, an improved transmission system, and programming designed to effectively utilize the power of two computer systems on a real-time basis.

## Introduction

Two of the major problems encountered within a large manufacturing plant are the control of manufacturing processes and the testing of products. These problems are often solved by providing custom control equipment for each isolated process and by designing and building custom test equipment for each product type. These solutions are generally expensive in terms of engineering effort required, the cost of the custom equipment itself, the time lag before the equipment can be operational, and the inflexibility of such equipment.

A Computer Operated Manufacturing and Test System (COMAT) has been designed and installed in IBM's San Jose manufacturing plant to replace the custom equipment with standard equipment. This has been accomplished by allowing a small, versatile, stored-program computer to act as the interface with a product or process through a minimal adapter. In order to keep these small computers inexpensive and yet maintain power and versatility, they are directly connected to a large-capacity, time-shared central computer which is programmed to supervise and service the terminals.

This systems concept has been referred to as a satellite system,<sup>1,11</sup> since the terminals are satellites on the central computer system (see Fig. 1). However, this concept should not be confused with another system configuration

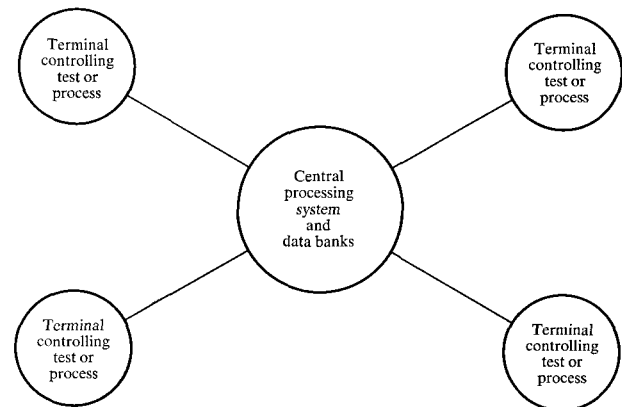
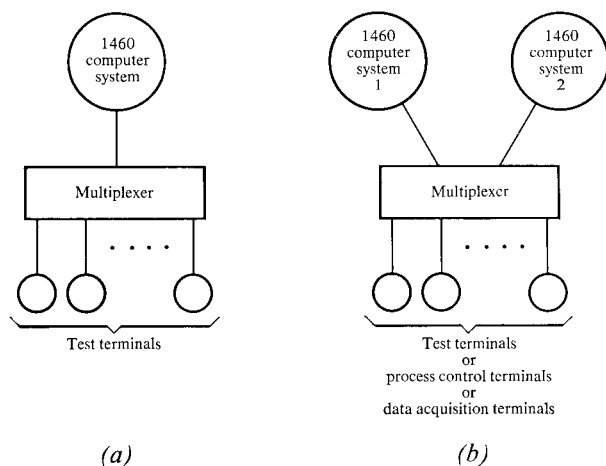


Figure 1 Satellite computer system concept.

which also is often referred to as a satellite system.<sup>2-4</sup> The latter is a central computer system providing a multiplicity of input and output lines (both analog and digital) directly to a variety of nonrelated processes, whereas the central computer of the COMAT satellite system supervises other computers (terminals) which in turn provide the direct interfacing and control.

The COMAT System has undergone two distinct phases of development. In Phase I the test terminal, multiplexer,



**Figure 2** Development of COMAT system; (a) Phase I, one central computer linked through multiplexer with terminals devoted exclusively to product test; (b) Phase II, two duplexed central computers linked through multiplexer with terminals for product test, process control, and data acquisition.

and a high-speed data transmission system were designed and implemented with a single IBM 1460 Data Processing System serving as the central computer system (Fig. 2a).

The test terminal is a special-purpose, stored-program computer which was designed to replace custom designed testers. The stored program provides the versatility that allows this objective to be realized. The multiplexer is the tool that allows many terminals to be connected to the central computer system. Basically, it is a large electronic switch capable of interconnecting any terminal to the central system for direct communication. The transmission logic was developed to allow any terminal to communicate with the central system at computer speeds (1.25 megabits/sec) over distances up to a mile over coaxial cable. The 1460 was chosen as the central system because of its processing ability and high-speed input/output equipment.\*

Phase II of the project (Fig. 2b) included the design of a new multiplexer, file control units, new transmission logic, a process control terminal, a data acquisition terminal, and implementation of a second (duplexed) 1460 system. The main reasons for undertaking Phase II were:

1. To provide a multiplexer with increased terminal capacity since the number of test terminals installed during Phase I had exceeded all expectations. The capacity was increased from 64 to 99 terminals.

\* We emphasize that the systems design decisions reported in this paper were made on the basis of alternatives available at the time of development. Thus, the IBM System/360 was not considered for use as the central processor in the COMAT installation at San Jose. Furthermore, the IBM 1800 Data Acquisition and Control System was not yet available at the time of development. It should also be recognized that the special terminals, as well as the multiplexer used in this system, are not part of the IBM product line.

2. Because of the large amount of testing and control dependent on the system, to provide 100% backup in case any common component (computer or multiplexer) of the system failed.

3. To provide additional computing power at the central system because of the increased terminal activity.

4. To provide file control units for a large-capacity (over 200 million characters) disk file system which may be accessed by either central computer.

In addition, the process control terminal was designed with the objective of using the central system concept to make it unnecessary to have many full scale computer systems within the plant controlling unrelated processes.<sup>5</sup> A data acquisition terminal was also designed in Phase II to utilize the processing power of the central computers and the large data storage bank. Basically, the data acquisition terminal acts as a buffer between the central system and any device (e.g., a computer) which can use the processing power of the central system or requires access to the data banks.

### Test terminal

The test terminal was designed to replace custom-built equipment used to test and exercise computer input/output devices such as disk files. The characteristics of custom test equipment that were considered undesirable included expense, engineering design effort, long lead times, high maintenance costs, obsolescence, lack of data recording capability, and resistance to product and test changes due to its inflexibility.

The dissatisfactions with custom test equipment in an environment of many and varied products led to the idea for developing a universal tester which could be easily modified for each new application. Such a universal tester would require only a one-time design and documentation effort. Since many universal testers would be built in place of several types of custom testers, quantity and standard build practices would lower the cost. Build and maintenance personnel would become proficient with exposure to only one tester, thus decreasing delivery time and maintenance down time. Universal testers removed from a phased-out product could be applied to a new product, alleviating the necessity of scrapping the testers while also decreasing the cost of test equipment for the new product.

In studying the requirements of such a universal tester, it was determined that the basic interface between the tester and the product under test should consist of output lines (voltage signals) which would be exercised in a sequence commanded by the input lines. Thus, the tester need only provide the sequence (state) logic which was the essence of the custom tester. A minimal adapter would provide the necessary interfacing between the tester and the unique product under test. To change the sequencing for

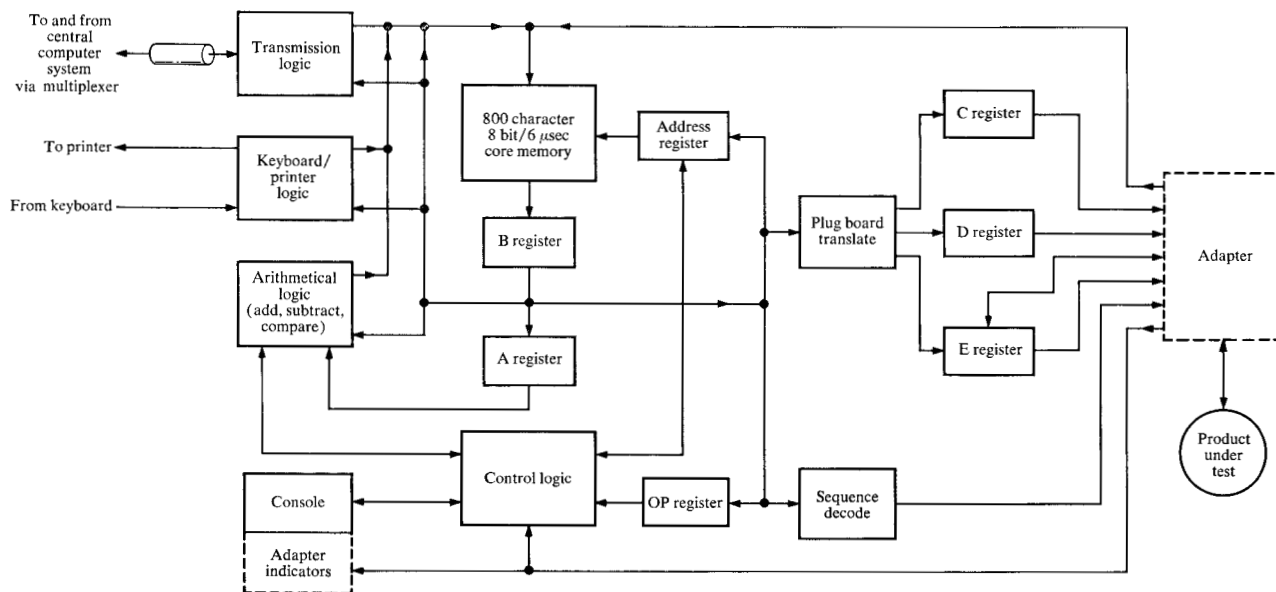


Figure 3 Block diagram of product test terminals.

different products and the mode of sequencing for a given product, it was determined that the tester should be easily programmable, i.e., a stored program device.

To provide this device at low cost, however, it is necessary that memory size be kept as small as possible. But if memory is smaller than the size needed to store a complete testing program, a means must be provided so that different parts of the program can be brought into the tester without delaying the test of a product. Card input (too slow) and tape, disk, or drum input (too expensive) were considered to be unsuitable means for making the programs available to the tester.

The solution which appeared to have many advantages was a central computer system having centrally located disk files. Such a system could provide any tester with a requested program within milliseconds. In addition, the central computer could accumulate test results and prepare reports. Thus, the universal testers became "terminals" (or satellites) on the central system. The central computer system will be discussed later.

With a solution in hand to the problem of input to the test terminals, further systems design indicated that the test terminal should have some logical capabilities (such as binary addition and subtraction and comparison) as well as a few registers on the interface to provide command and control information to the adapter. These capabilities made the test terminal even more versatile and decreased to a minimum the amount of unique logic to be provided by an adapter to the product under test.

The next problem to be solved in designing the test

terminal was the interface between the unit and the technician controlling the test. On the custom testers, complex mazes of indicators, displays, and switches were used by the technician to change test phases and monitor test results. It was decided that a simpler interface to the operator would be a keyboard/printer. A scheme of operation was defined in which the operator keys in a program request which is sent to the central computer for analysis. The test terminal begins the test after receiving its program from the central computer. It then monitors the test, compares limits, and prints out results for the operator. A selection of "sense switches" permits the operator to change modes of testing within the same program. A special panel is provided on the console to allow an adapter control panel which may contain any special displays or controls required by the specific product.

The block diagram of the test terminal is shown in Fig. 3. The memory is buffered by the B (buffer) register which provides data to all parts of the test terminal. The "A" register holds one operand in arithmetic and logical operations. The C, D, and E registers are output registers to the adapter and are loaded from memory through a manually programmed plugboard which permits versatility in the bit configuration (e.g., binary, octal, or BCD code). The "E" register is also a binary counter which may be incremented by the adapter. All of the described registers are eight bits long. The sequence decode provides sequencing or state lines to the adapter by decoding characters as they are read from memory on certain instructions. There are 36 such lines. An eight bit

bus is provided the adapter for reading data into memory. The instruction set and data flow of the test terminal are similar to those of the IBM 1441 Central Processing Unit in a very restricted sense.

### Process control terminal

While the implementation of the central computer concept for the purpose of product tests appeared justified for that purpose alone, another possible use for the COMAT system was recognized. There are many high-volume components and subassemblies used in IBM products which require sophisticated manufacturing and testing processes. These complex processes require constant (real-time) monitoring and control. The approach adopted for the control of such processes<sup>6-9</sup> has usually been one of three alternatives: custom control, paper-tape numerical control, or direct digital-computer control. But, for the observed applications, a controller unique to a given process was unsuitable for many of the same reasons that a custom tester was not desirable. Another possibility, the use of leased or purchased numerical control devices, was also judged unsuitable, primarily for economic reasons. Also, the use of either the customized or numerically controlled devices would have precluded any automatic reporting of production and product quality data. A third approach could have been the use of a computer system that would interface directly with the various processes to be controlled. Although a control computer of this type has the desired automatic reporting capability, any time it spends in preparing reports is production time lost. Furthermore, it was thought that the necessity for maintenance of the associated input-output equipment could contribute to excessive downtime.

To overcome the disadvantages of the conventional approaches to controlling a number of complex, high volume manufacturing processes, a standard, very versatile and reliable process controller with reporting capabilities was proposed. The requirements of versatility and report generation specified that the standard process controller be a stored-program computer. However, for ultimate reliability, the computer should not have any mechanical input/output devices tied directly to it. Thus, it appeared that the central processing unit from some computer system might be modified by providing a process control interface. The processing unit could then be attached to the already existing COMAT System for input/output and report generation.

The processing unit chosen for the process control terminal was the IBM 1441 Central Processing Unit. This unit has several advantages, the main one being its compatibility with the 1460 System which served as the central computer. Other advantages included low cost, high speed, programming support and ease of maintenance.

Several existing processes were studied, as were processes in the design stage, to determine the interface requirements to a typical IBM manufacturing process. It was decided that the process controller should be modularly equipped with latching contact operate (latches which may be set or reset by program), momentary contact operate (electrical pulses initiated by the program), contact sense (input voltage lines which may be sensed by the program), high-speed digital input/output channels (data channels for transfer of information between memory and the process), interrupt (the ability to interrupt the program to obtain immediate service), and interval timers (counters with the ability to interrupt the program at the end of a given interval of time or after a given count of pulses from the process). Space for an adapter was provided the user for any unique interfacing problems he might have, including analog input and/or output. A process control terminal having these features was implemented and made a part of the COMAT system.

### Data acquisition terminal

A third type of terminal unit was installed on the COMAT system to take advantage of the large-capacity files and the processing capability of the central computers. The two terminals previously described were both stored program processors. However, a need existed for a very inexpensive and unsophisticated terminal which would, in effect, do nothing more than act as an input/output buffer to the central computer system.

Within the plant there was still a need for some very specialized test equipment (e.g., precision component testing and commercial test equipment) which contained its own control. However, it was determined that a great savings would be realized if such equipment could be interfaced with the central computer system, which would act as a data collection point. The central processors could collect data from the test equipment, analyze it, store test results, print reports and send back to the test area (via a printer terminal) test results in graphical form.

The terminal could also provide access to the large centrally located files. When a computer system's central processing unit is tested, many large programs are fed into the processor via a card reader. The buffer unit could provide the processor under test with access to programs stored at the central computer system, thereby eliminating the need for the card reader and large quantities of punched cards. Thus, the data acquisition terminal was designed to consist of little more than the necessary transmission logic to interface with the central computer system, a buffer and control logic. The buffer was optionally 800 eight-bit characters (or 400 sixteen-bit characters) in core storage or, in the case of high-speed applications, a single register. The output from the buffer was hardware programmable to be three-bit octal, four-bit BCD, eight-bit

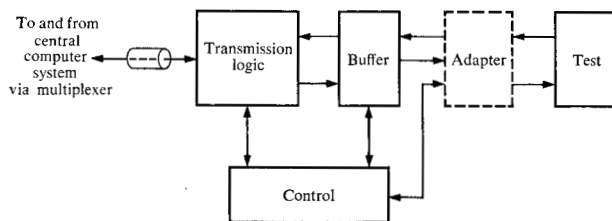


Figure 4 Block diagram of data acquisition terminal.

BCD, or sixteen-bit hexa-decimal. An adapter would then be used to interface the data acquisition terminal with the unique application. The block diagram of the terminal is shown in Fig. 4.

### Multiplexer

The preceding Sections have discussed the considerations on which the development of three types of terminals for the COMAT system was based. Equally important in implementing the system was the need for a means to control the flow of data being transmitted between the central computers and the various terminals. The design of a multiplexer to do this was predicated on the following requirements:

1. The input/output channel of either of two central computers must be switchable to any one of 99 terminals to allow direct communication.
2. Any one of the terminals must be able to initiate an interrupt at the central system to ask for programs, transmit data, or report status. A terminal-initiated interrupt must always be answered by a central processor if only to report that data have been received.
3. Either central processor must be able to initiate a call to any individual terminal. Such calls could be to transmit queued messages, inquire about status, or send back processed results from an earlier transmission.
4. Since the terminals can request service randomly and either central processor may answer, the time of the request must be recorded in order to keep sensible history records. Therefore, a real-time clock is required which is accessible to either processor.
5. A bulk-storage disk file system is required which may be accessed by either central processor. These files are used to store the large quantities of programs and data needed by the terminals. The access must be common in order that both central processors have the ability to service any terminal.
6. Reliability is a prime consideration since all terminals would be without service should the system fail. Therefore, all common components of the system should be backed up.

Thus, the multiplexer was defined to provide channel switching, initiate bidirectional interrupts, and provide the real-time clock and file control units. A simplified functional schematic of the multiplexer is shown in Fig. 5.

As indicated in the schematic, two ninety-nine position switches are used to interconnect any terminal with either processor. In addition, a third ninety-nine position switch is used for "scanning." The function of the scanner switch is to poll in succession each terminal to determine its status. When the scanner detects a terminal requesting service it assigns that terminal to central computer 1 if that computer is interruptable. If computer 1 is not interruptable (busy or off line), the terminal is assigned to computer 2. If computer 2 is not interruptable, the scanner will wait until one of the two computers becomes available. Two scanners are provided in the multiplexer to allow backup in the event one scanner fails.

The scanner normally assigns an interrupt to computer 1 (if interruptable) because that computer is the main processor in the duplexed configuration. Computer 2 (the standby processor) will be interrupted only if computer 1 is busy (not highly probable) or off line for maintenance. Thus, computer 2 can more effectively be utilized for time-shared processing. That is, all program assemblies, special production reports, and other similar programs will be run on the standby processor where the most time is available. If computer 2 is interrupted, the time-shared processing will be discontinued until the servicing of interrupts is completed.

In order to facilitate the phasing-in of new terminals without affecting the on-line system, provision was made to switch any terminal to only one of the two central computers. For example, if a new terminal were being installed on channel 82, this channel could be switched to computer 2 and all other terminals switched to computer 1 to handle the normal servings. Thus, the scanner would never assign a terminal to computer 2 except the terminal on channel 82.

Once a terminal has been assigned to one of the two computers, the scanner is free to continue polling. The multiplexer channel unit now completes the job by requesting the terminal to transmit its message. The message is given to the computer that answers the request via the multiplexer channel. Thus, one computer and its associated channel are busy during the entire servicing of an interrupt (normally about one second); however, the other computer and channel may be servicing another terminal. Since both computers and their associated channels are isolated from each other, 100% backup is provided.

Designed in each multiplexer channel is the ability to initiate a CPU (Central Processing Unit) call. The central computer gives the multiplexer the address of the terminal it wishes to communicate with and the channel initiates an interrupt to the terminal. The channel then transmits the

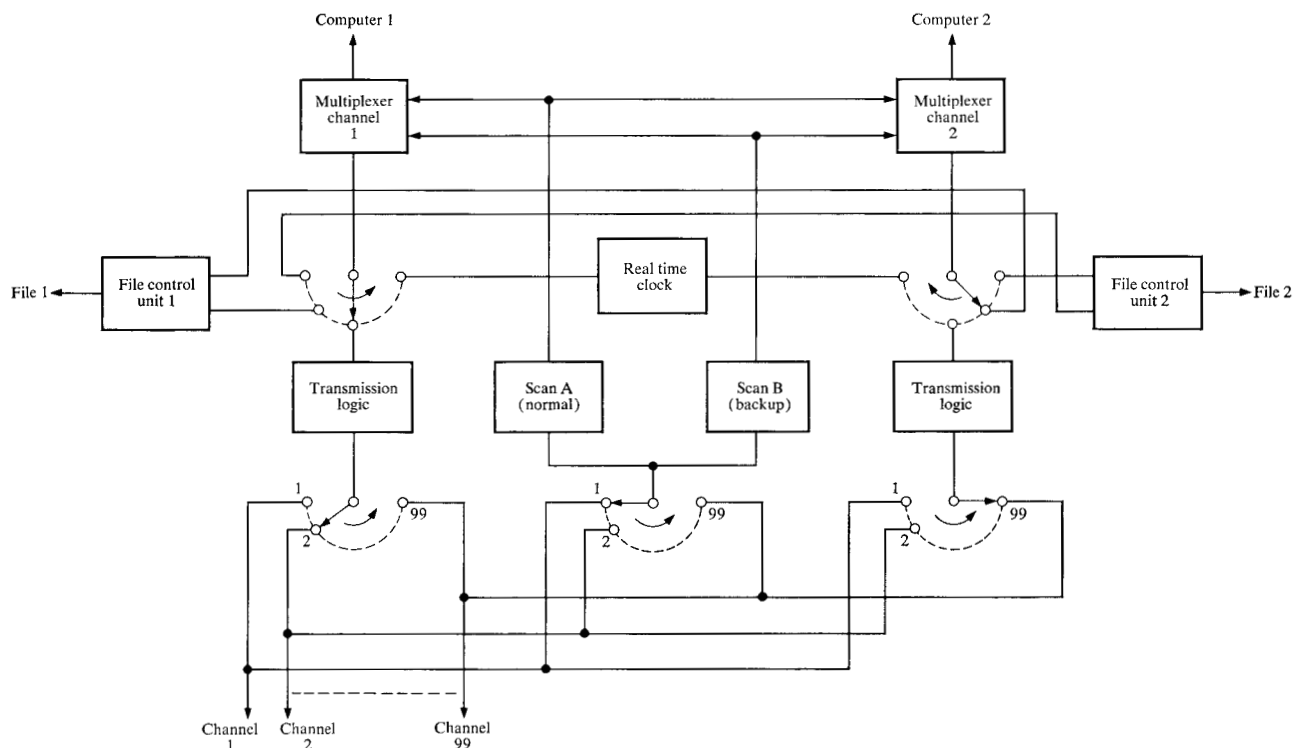


Figure 5 Simplified schematic of multiplexer.

data from the computer to the terminal unit (no answer back from the terminal is expected). If the terminal is off-line or busy, the computer will be so informed, thus allowing the message to be queued for that terminal.

In addition to the terminal switching logic, the multiplexer provides two separate file control units each of which may be accessed by either central computer. One file control unit contains all the logic necessary for addressing, reading, and writing on an IBM 2302 Disk File (234 million character capacity). The other file control unit contains similar logic for controlling an IBM 1311 Disk File (two million character disk pack). The 2302 File contains manufacturing data such as that required by process control terminals controlling numeric equipment. This file is backed up by utilizing either central computer's 1311 Disk File (the system configuration will be described later). Although the 1311 has considerably less capacity than the 2302, it can be used to provide data for the most important processes.

The shared 1311 File is used to accumulate history records and test results which might be acquired by either central processor. This file is backed up by the 1311 File on one of the central processors. When either shared file (or control unit) is down for maintenance, the system operates in a simplex configuration (one computer completely off line).

The multiplexer also provides a digital real-time clock which is accessible to either central computer. A computer normally reads and records the time (in seconds, hour, day, month and year) when executing any terminal transaction.

#### Central processor configuration

The computer system chosen to serve as central processor was the IBM 1460 Data Processing System. At the time, this system appeared to be an optimum choice because of its processing ability, powerful I/O devices, its BCD language, programming simplicity, and the overall cost.\* Two computer systems were specified for the reasons given in the Introduction of this paper. The central processor configuration is shown in Fig. 6.

The only difference in the two computers' configurations is that computer 2 has three additional tape drives. These additional drives are to allow that processor (the standby processor) to perform sorts and other data processing activities on a time-shared basis. The rest of the I/O equipment serves the same purpose on each computer. The 1441 is the central processing unit, which contains the core memory, arithmetic logic and instruction logic. The SIO (serial input/output) channel on the 1441 is utilized to

\* A study is currently under way to determine the feasibility of replacing the 1460's with an IBM System/360. The justification for the study lies primarily in the faster processing time of the 360 and the increased storage capacity.

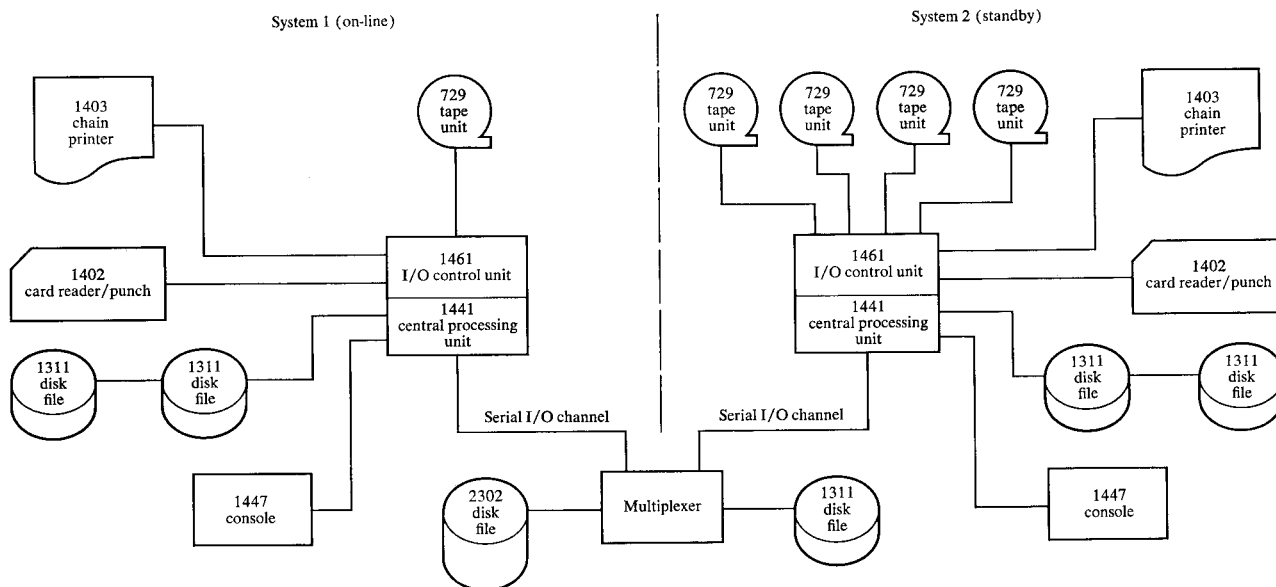
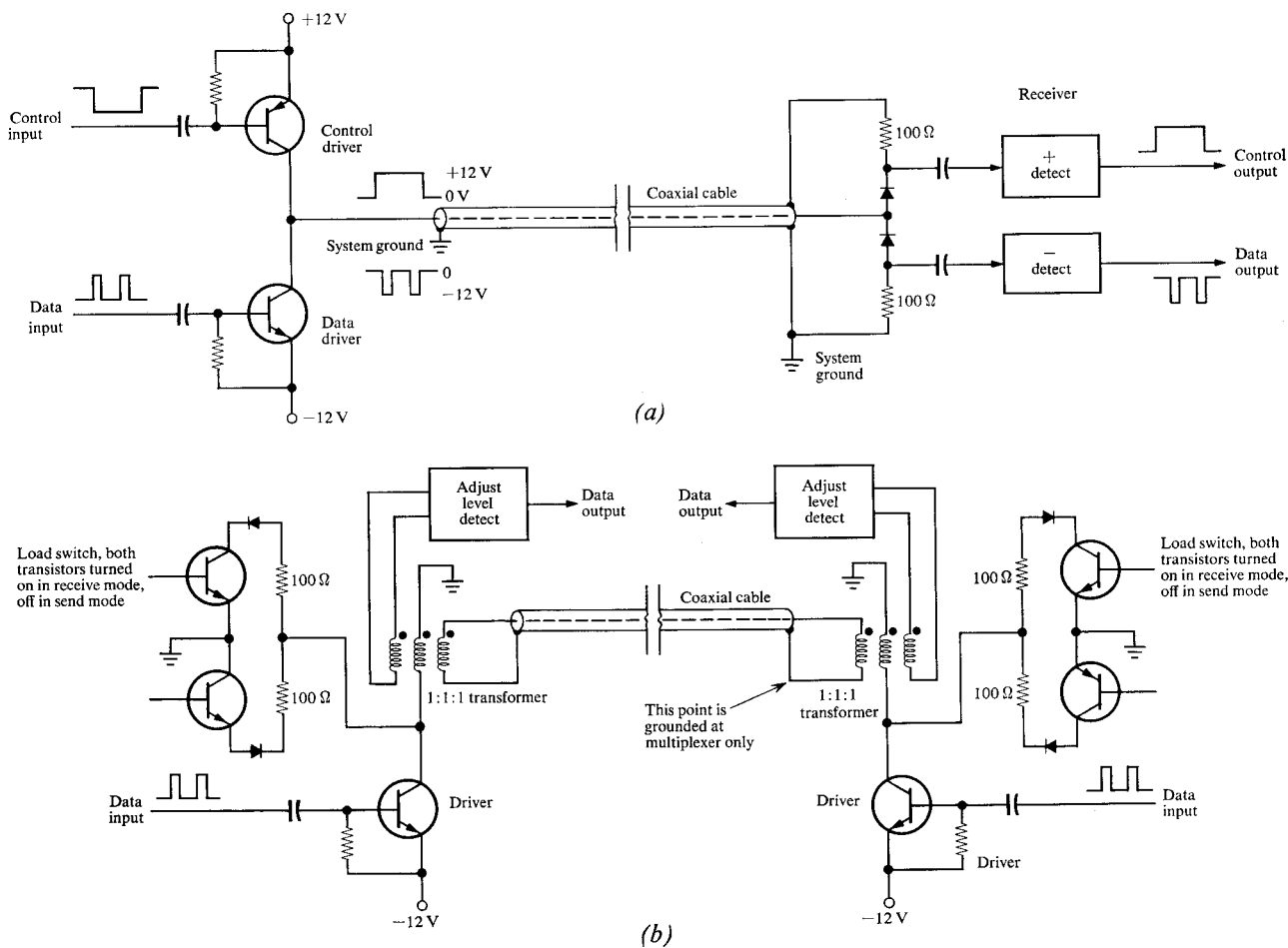


Figure 6 Central processor configuration.

Figure 7 High-speed data transmission system; (a) early version; (b) improved version.



provide interfacing between the processor and multiplexer. The 1461 is an I/O Control Unit which interconnects the Card Reader/Punch, the Printer, and the Tape Units with the Central Processing Unit.

The 729 Tape Unit is used to store terminal requests (along with the time). The 1403 Printer is used to prepare printed output reports. The 1402 provides card input to the system and card output when required. One 1311 File is used to store terminal programs and the second is for backup and time shared processing. The purpose of the shared 1311 and 2302 Files on the multiplexer has been described in the preceding Section. The 1447 is the operator console and is equipped with a keyboard/printer for manual input and output.

### High-speed data transmission system

In order for the satellite system concept to be effective on a real-time basis it was necessary to develop a transmission system which would allow the terminal units to communicate with the central computer at a computer rate of speed (approximately 6  $\mu$ sec/character). The real technical problem was to achieve this rate of transmission over distances up to one mile, without repeaters, in an electrically noisy manufacturing atmosphere. These two requirements prevailed during the design of both Phase I and Phase II of the system. The Phase II redesign of the High-Speed Data Transmission System (HSDTS) was undertaken to correct some problems which were encountered during the time Phase I was operational.

The Phase I HSDTS had the following operational characteristics:

|                             |                                                                                                                                        |
|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| <i>Maximum range:</i>       | One mile without repeater amplifiers.                                                                                                  |
| <i>Speed:</i>               | 133,000 characters/sec (slightly less than 6 $\mu$ sec/char to allow the HSDTS to synchronize the terminal with the central computer). |
| <i>Transmission mode:</i>   | Half duplex, synchronous transmission, serial by bit and serial by character.                                                          |
| <i>Character format:</i>    | Eight data bits plus two control bits.                                                                                                 |
| <i>Clocking:</i>            | Double frequency (10 clock bits/char).                                                                                                 |
| <i>Transmission medium:</i> | Two flexible coaxial cables (one for each direction of transmission), each direct-coupled at both ends.                                |

The HSDTS consisted of the following functional components: (1) Serializer-deserializer (to convert serial bits to characters and vice versa), (2) buffer register (to buffer

incoming and outgoing data), (3) interface controls (to synchronize the transmission logic with the memory being read into or out of), (4) timing circuitry, and (5) transmission line, line drivers, and line terminators. The first four of these components are common digital data handling functions that are not considered unique in any respect so will not be discussed in this paper. The transmission line, line drivers, and line receivers, shown in simplified form in Fig. 7a are unique and were the cause of the technical problems encountered during Phase I. These problems were:

1. Common mode noise or ground shift, such as power line transients which are very common in a factory environment, caused an intolerable number of transmission failures. Direct coupling between the terminals and the central system was largely responsible for this trouble, but the dc signals used for control were also considered contributors.
2. The data signal transmitted in this system contained dc as well as ac components. Because the coaxial cable attenuation is less at dc than it is at the pulse repetition frequency, the signal suffered a base line shift which increased with cable length. This effect was compensated for, with some success, by using R-C networks. However, tests indicated that elimination of the dc component from the signal would solve this problem completely.

To overcome these problems, the HSDTS was redesigned and implemented during the second phase of the system. The redesign also provided the economy of needing only a single coaxial cable for transmission in both directions. The following design requirements were established for this second HSDTS:

|                             |                                                                         |
|-----------------------------|-------------------------------------------------------------------------|
| <i>Maximum range:</i>       | One mile without repeater amplifiers.                                   |
| <i>Speed:</i>               | 125,000 eight-bit characters/second.                                    |
| <i>Transmission mode:</i>   | Synchronous transmission, serial by character and serial by bit.        |
| <i>Character format:</i>    | Eight data bits plus two control bits.                                  |
| <i>Clocking:</i>            | One clock bit per character.                                            |
| <i>Transmission medium:</i> | A single flexible coaxial cable with transformer coupling at both ends. |

Figure 7b is a simplified drawing of this system. Transformer coupling was the key to the solution of both problems stated above. Selection of a transformer with low interwinding capacitance and balanced windings minimized common mode noise problems and provided dc isolation between the multiplexer and terminals. The specification



of a narrow band pass at a high frequency in the transformer effectively eliminated the dc and low frequency components of the signal which solved the base line shift problem. This application imposed another restriction on the transformer; transformer inductance and line impedance must provide an L/R time constant small enough so that the transformer core has time to recover between pulses. However, it must be large enough so that the circuit is adequately damped and the driver transistor is not damaged by the recovery transient.

The new HSDTS is operative on the Phase II system and has apparently solved all of the problems encountered during Phase I. The approximate reliability in the electrically noisy manufacturing plant is  $10^{-8}$  bit failures.

### Conclusions

Phase 1 of the COMAT system was operative in January 1965 with three test terminals on line. By the middle of 1965, with twenty terminals on line, projections indicated that Phase II development must get underway as forecast applications had increased considerably. Phase II was operative May 1966. At present, the terminal configuration includes 60 test terminals which are testing fourteen different IBM products. In addition, 18 process control terminals are installed for operating various manufacturing and testing processes. Eight data acquisition terminals are installed as buffers for final testing computers and interfacing to other test equipment. At the present time a new 200-channel multiplexer is being designed to allow for further growth.

The operating system was simulated<sup>10</sup> by a 7094 computer. The simulation assumed 64 terminals on line with a mean interval between arrival of interrupts of 5.4 sec. The results of the simulation (which closely approximated the observed results) indicated that the mean waiting time for any terminal to be serviced was 1.54 sec. The maximum queue of terminals waiting for service at any time was 2, and 99.9% of the time there was no waiting. Observations indicate that the system is operative on a 24 hour/day, seven day/week basis 99.7% of the time.

The design objectives of the system have been fully met. Cost of equipment, design time, maintenance time and even test time have all been significantly decreased. The objective of versatility is best described by an example. In the past, if new test stations were required for a product undergoing production expansion, new test equipment would have to

be ordered. The delay in making the equipment operational was generally at least three months. It was requested that production on one of the products being tested on the COMAT system be expanded. This meant increasing the number of test stations by four. Within one week two test stations had been added by removing test terminals from a product which did not have such a heavy schedule. The next week two additional test terminals were obtained in a similar manner from another product. Thus, production was effectively increased within two weeks instead of three months.

### Acknowledgments

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